Amendments to the Claims:

Re-write the claims as set forth below. This listing of claims will replace all prior versions and listings, of claims in the application:

Listing of Claims:

1. (Canceled)

2. (Previously Presented) The method of claim 21, wherein the first portion and the second portion are the same portion.

3-5. (Canceled)

6. (Previously Presented) The method of claim 21, wherein the first video memory and second video memory are accessed by a direct memory access (DMA) controller associated with the first VGA.

7. (Previously Presented) The method of claim 21, wherein the first video memory and second video memory are accessed by a direct memory access (DMA) controller on the second VGA.

8. (Previously Presented) The method of claim 21, wherein the first VGA is a primary VGA, and the second VGA is a secondary VGA.

9. (Previously Presented) The method of claim 21, wherein the first VGA is a secondary VGA, and the second VGA is a primary VGA.

10. (Previously Presented) The method of claim 21, wherein the first VGA and the second VGA are part of a video wall such that the first frame of active video is displayed across multiple displays simultaneously.

11. (Previously Presented) The method of claim 21 further comprising the steps of:

receiving at the second VGA a second frame of active video from a second video source; and

rendering at least a portion of the second frame of video at the first VGA.

12. (Canceled)

13. (Previously Presented) The method of claim 21 further comprising the step of storing the window location in a preference file.

14-16. (Canceled)

17. (Previously Presented) The method of claim 22, wherein the video decoder is for decoding a compressed video signal.

18. (Previously Presented) The method of claim 22, wherein the method further comprises the video source sending the first frame of data over a bus local to the first VGA.

19.-20. (Canceled)

21. (Currently amended) A method of displaying active video on a computer system, the method comprising the steps of:

receiving at a first video graphics adapter (VGA) a first frame of active video from a video source;

rendering at least a first portion of the first frame of active video at the first VGA in response to a first control signal, wherein the first control signal is a signal specifying a window location for displaying the active video;

storing at least a first portion of the active video in a video memory in a memory location mapped to the first VGA; [[and]]

rendering at least a second portion of the first frame of video at a second VGA in response to a second control signal and storing at least the second portion of the active video in a video memory in a memory location mapped to the first VGA; and

sending the first frame of data over a local bus of the first VGA and the first video graphics adapter sending a portion of the first frame for the second video graphics adapter via a non-local bus.

22. (Currently amended) A method of displaying active video on a computer system, the method comprising the steps of:

receiving at a first video graphics adapter (VGA) a first frame of active video from a video source, wherein the video source is at least one of the following: a video decoder and a television signal;

storing the first frame of active video in a video memory in a memory location mapped to the first VGA; [[and]]

displaying at least a first portion of the first frame of video at a second VGA in response to a second control signal, wherein the second control signal is a signal specifying a window location for displaying the active video; and

wherein storing the first frame of active video in the video memory includes locally accessing the video memory by the first VGA.

23. (Currently amended) An active video processing system comprising:

a first video graphics adapter (VGA) operative to receive a first frame of active video data, and in response display at least a first portion of the first frame of active video data at a window location in response to a first control signal;

a first video memory having a memory location mapped to the first VGA and operative to store at least the first portion of the active video data;

a second VGA, operatively coupled to the first VGA and operative to receive the at least a second portion of the first frame of active video data, and in response to display at least the second portion of the first frame of active video data; [[and]]

a second video memory having a memory location mapped to the second VGA and operative to store at least the second portion of the active video data; and

wherein the first video memory is locally accessible by the first VGA and wherein the second video memory is locally accessible by the second VGA.

24. (Previously Presented) The active video processing system of claim 23, wherein the first VGA receives the first control signal when the first VGA receives a command to display at least the second portion of the first frame of active video data on the second VGA.

25. (Previously Presented) The active video processing system of claim 23, wherein the first VGA further includes a video graphics processor, and the second VGA further includes a video graphics processor.

26. (Previously Presented) The active video processing system of claim 23, wherein the window operates in conjunction with an operating system, such that the operating system supports the display of the active video data on the first VGA.

27. (Previously Presented) The active video processing system of claim 23, wherein the window operates in conjunction with an operating system, such that the operating system supports a program for providing the active video data only to the first VGA.

28. (Previously Presented) The active video processing system of claim 23, wherein the first portion and the second portion are the same portion.

29. (Previously Presented) The active video processing system of claim 23, further including a direct memory access (DMA), wherein the first video memory and second video memory are accessed by a direct memory access (DMA) controller associated with the first VGA.

30. (Previously Presented) The active video processing system of claim 23, further including a direct memory access, wherein the first video memory and second video memory are accessed by the DMA's controller associated with the second VGA.

31. (Previously Presented) The active video processing system of claim 23, wherein the first VGA is a primary VGA, and the second VGA is a secondary VGA.

32. (Previously Presented) The active video processing system of claim 23, wherein the first VGA is a secondary VGA, and the second VGA is a primary VGA.

33. (Previously Presented) The active video processing system of claim 23, wherein the first VGA and the second VGA are part of a video wall, such that the first frame of active video is displayed across multiple displays simultaneously.

34. (Previously Presented) The active video processing system of claim 23 further comprising the steps of:

receiving at the second VGA a second frame of active video from a second video source; and

rendering at least a portion of the second frame of video at the first VGA.

35. (Canceled)

36. (Previously presented) The method of claim 21 including storing at least a first portion of the active video in the video memory by accessing the video memory locally by the first VGA and storing at least the second portion of the active video in the video memory accessed locally by the first VGA.

37. (Canceled)

38. (Canceled)